CLAIMS

WHAT IS CLAIMED IS:

1. A method of fabricating a non-volatile semiconductor memory device comprising:

forming a charge storage layer on a substrate;

forming a control gate layer on the charge storage layer;

forming a gate mask in the shape of a spacer on the control gate layer; and

removing the charge storage layer and the control gate layer, wherein the gate mask protects a portion of the charge storage layer and the control gate layer to form a control gate and a charge storage region.

2. The method of claim 1, wherein forming the gate mask comprises:

forming a disposable pattern on the control gate layer;

forming a gate mask layer on the disposable pattern and the control gate layer; and

removing a portion of the gate mask layer to form a gate mask on a sidewall of the disposable pattern.

3. The method of claim 2, wherein removing the charge storage layer and the control gate layer comprises:

etching the charge storage layer and the control gate layer using the gate mask and the disposable pattern as a etching mask thereby protecting a portion of remaining the charge storage layer and the control gate layer under the gate mask and the disposable pattern;

removing the disposable pattern; and

etching the remaining portion of the charge storage layer and the control gate layer using the gate mask as an etching mask thereby forming a control gate and a charge storage region under the gate mask.

4. The method of claim 3 further comprising:

forming a source in the substrate adjacent to a sidewall of the control gate; and

forming a source-side spacer on the sidewalls of the control gate and the charge storage region;

forming a source electrode on the source, wherein the source electrode is isolated from the control gate and the charge storage region by the source side spacer.

5. The method of claim 1 further comprising forming a select gate on a sidewall of the charge storage region.

6. The method of claim 5, wherein the select gate is in the shape of a spacer.

7. The method of claim 5 further comprising:

forming an LDD region in the substrate using the select gate as a LDD implantation mask; and

forming a LDD spacer on a sidewall of the select gate.

8. The method of claim 1, wherein forming the charge storage layer comprises:

forming a floating gate dielectric layer on the substrate;

forming a floating gate layer on the floating gate dielectric layer; and

forming an inter poly dielectric layer on the floating gate layer.

9. The method of claim 1, wherein forming the charge storage layer comprises forming an ONO layer on the substrate.